TS512MSK64V3N-I

204PIN DDR3 1333 SO-DIMM
2Rank 4GB With 256Mx8 CL9

Description

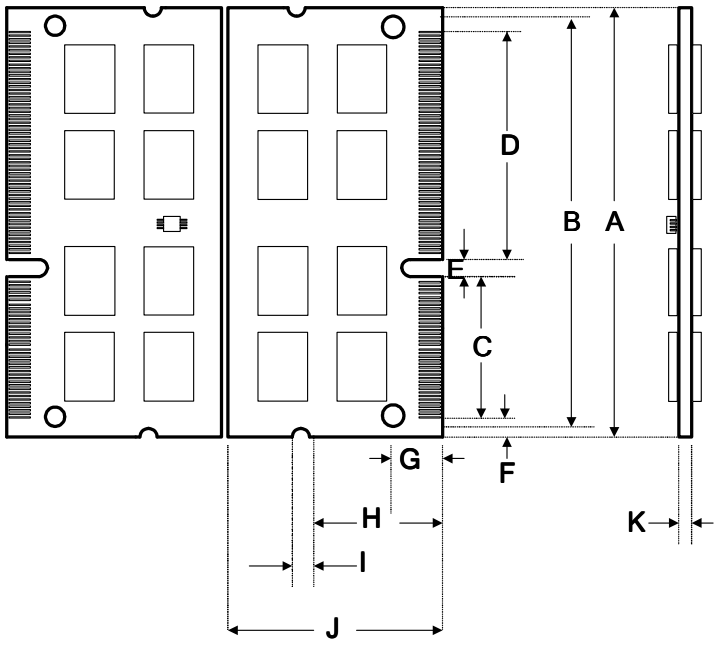
The TS512MSK64V3N-I is a 512M x 64bits DDR3-1333 2Rank SO-DIMM. The TS512MSK64V3N-I consists of 16pcs 256Mx8bits DDR3 SDRAMs FBGA packages and a 2048 bits serial EEPROM on a 204-pin printed circuit board. The TS512MSK64V3N-I is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Operating Temperature : -40°C to +85°C
- Gold plating of PCB gold finger is 30u
- RoHS compliant products.
- JEDEC standard 1.5V ± 0.075V Power supply
- VDDQ=1.5V ± 0.075V
- Clock Freq: 667MHZ for 1333Mb/s/Pin.
- Programmable CAS Latency: 6, 7, 8, 9
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 7 (DDR3-1333)
- 8 bit pre-fetch
  Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

■ Placement



PCB: 09-2841

Dimensions

Side	Millimeters	Inches
A	67.60±0.15	2.661±0.006
B	63.60	2.503
C	22.38	0.881
D	40.08	1.578
E	1.00	0.039
F	2.15±0.15	0.085±0.006
G	6.00	0.236
H	18.00	0.709
I	4.00	0.157
J	30.00	1.181
K	1.0±0.1	0.039±0.004

(Refer Placement)

Pin Identification

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	DIMM Rank Select Lines.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Voltage power supply
VDDQ	Voltage Power Supply for DQS
V_{REF}DQ/ V_{REF}CA	Power Supply for Reference
VDDSPD	SPD EEPROM Power Supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	69	DQ27	137	DQS4	02	VSS	70	DQ31	138	VSS
03	VSS	71	VSS	139	VSS	04	DQ4	72	VSS	140	DQ38
05	DQ0	73	CKE0	141	DQ34	06	DQ5	74	CKE1	142	DQ39
07	DQ1	75	VDD	143	DQ35	08	VSS	76	VDD	144	VSS
09	VSS	77	NC	145	VSS	10	DQS0	78	A15	146	DQ44
11	DM0	79	BA2	147	DQ40	12	/ DQS0	80	A14	148	DQ45
13	VSS	81	VDD	149	DQ41	14	VSS	82	VDD	150	VSS
15	DQ2	83	A12	151	VSS	16	DQ6	84	A11	152	/DQS5
17	DQ3	85	A9	153	DM5	18	DQ7	86	A7	154	DQS5
19	VSS	87	VDD	155	VSS	20	VSS	88	VDD	156	VSS
21	DQ8	89	A8	157	DQ42	22	DQ12	90	A6	158	DQ46
23	DQ9	91	A5	159	DQ43	24	DQ13	92	A4	160	DQ47
25	VSS	93	VDD	161	VSS	26	VSS	94	VDD	162	VSS
27	/DQS1	95	A3	163	DQ48	28	DM1	96	A2	164	DQ52
29	DQS1	97	A1	165	DQ49	30	/RESET	98	A0	166	DQ53
31	VSS	99	VDD	167	VSS	32	VSS	100	VDD	168	VSS
33	DQ10	101	CK0	169	/DQS6	34	DQ14	102	CK1	170	DM6
35	DQ11	103	/CK0	171	DQS6	36	DQ15	104	/CK1	172	VSS
37	VSS	105	VDD	173	VSS	38	VSS	106	VDD	174	DQ54
39	DQ16	107	A10/AP	175	DQ50	40	DQ20	108	BA1	176	DQ55
41	DQ17	109	BA0	177	DQ51	42	DQ21	110	/RAS	178	VSS
43	VSS	111	VDD	179	VSS	44	VSS	112	VDD	180	DQ60
45	/DQS2	113	/WE	181	DQ56	46	DM2	114	/CS0	182	DQ61
47	DQS2	115	/CAS	183	DQ57	48	VSS	116	ODT0	184	VSS
49	VSS	117	VDD	185	VSS	50	DQ22	118	VDD	186	/DQS7
51	DQ18	119	A13	187	DM7	52	DQ23	120	ODT1	188	DQS7
53	DQ19	121	/CS1	189	VSS	54	VSS	122	NC	190	VSS
55	VSS	123	VDD	191	DQ58	56	DQ28	124	VDD	192	DQ62
57	DQ24	125	TEST	193	DQ59	58	DQ29	126	VREFCA	194	DQ63
59	DQ25	127	VSS	195	VSS	60	VSS	128	VSS	196	VSS
61	VSS	129	DQ32	197	SA0	62	/DQS3	130	DQ36	198	/EVENT
63	DM3	131	DQ33	199	VDDSPD	64	DQS3	132	DQ37	200	SDA
65	VSS	133	VSS	201	SA1	66	VSS	134	VSS	202	SCL
67	DQ26	135	/DQS4	203	Vtt	68	DQ30	136	DM4	204	Vtt